Notice of Allowability	Application No.	Applicant(s)	
	10/613,128	WILSON ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *7/27/2006*.

2. ☒ The allowed claim(s) is/are *1-6,10-15 and 23-26*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

GUY LAMARRE
PRIMARY EXAMINER

8/29/06

REASONS FOR ALLOWANCE

Claims 1-6, 10-15 and 23-26 are allowed. The following is an Examiner's statement of reasons for allowance:

Independent claim 1 of the present application teaches a processor for convolutional decoding, said processor embodying a pipelined superscalar processor core, comprising: an instruction prefetch unit, the instruction prefetch unit configured to simultaneously fetch first and second Viterbi instructions and to partially decode and align the first and second Viterbi instructions; an instruction sequencing unit, the instruction sequencing unit configured to fully decode the partially decoded first and second Viterbi instructions and to group the fully decoded first and second Viterbi instructions for simultaneous execution; a first processing unit for executing the first Viterbi instruction, the instruction sequencing unit issuing the first Viterbi instruction to the first processing unit; a second processing unit for executing the second Viterbi instruction, the instruction sequencing unit issuing the second Viterbi instruction to the second processing unit; a register comprising a plurality of ordered bit positions; and update logic coupled to the register, the first processing unit and the second processing unit, the update logic configured to receive a first signal indicative of a result of a first add-compare-select instruction from the first processing unit and a second signal indicative of a result of a second add-compare-select instruction from the second processing unit, the update logic further configured to update the contents of the register dependent upon the first and second signals; wherein, in the event that: (1) the first signal but not the second signal, or (2) the second signal but not the first signal, is received, the update logic is configured to shift the contents of the register such that one bit position is vacated and to update the vacated bit position dependent on the received signal; and

wherein the event the first and second signals are received substantially simultaneously, the update logic is configured to shift the contents of the register 2 bit positions in order thereby vacating 2 consecutive bit positions, to update one of the vacated bit positions dependent upon the first signal, and to update the other vacated bit position dependent upon the second signal. The foregoing limitations are not found in the prior arts of record. Particularly, none of the prior arts of record teach nor fairly suggest, "...an instruction prefetch unit, the instruction prefetch unit configured to simultaneously fetch *first and second Viterbi instructions and to partially decode and align the first and second Viterbi instructions*; an instruction sequencing unit, the instruction sequencing unit configured to fully decode the partially decoded first and second Viterbi instructions and to group the fully decoded first and second Viterbi instructions for simultaneous execution; ...*the update logic is configured to shift the contents of the register 2 bit positions in order thereby vacating 2 consecutive bit positions, to update one of the vacated bit positions dependent upon the first signal, and to update the other vacated bit position dependent upon the second signal.*"

Independent claim 10 includes similar limitations of independent claim 1 and therefore is allowed for similar reasons.

Dependent claims 2-6, 11-15 and 23-26 depend from allowable independent claims 1 and 10 and inherently include limitations therein and therefore are allowed as well.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
August 29, 2006

GUY LAMARRE
PRIMARY EXAMINER